

# Capital Budgeting, Coordination, and Strategy: A Field Study of Interfirm and Intrafirm Mechanisms<sup>1</sup>

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## Introduction

There has been remarkably little systematic study of the processes and practices through which capital budgeting decisions are made within and between organizations. The complex strategic and organizational phenomena created by capital budgeting have been similarly neglected. Such issues have fallen between the gaps that separate the distinct yet related literatures of accounting, finance, and strategy. Recent large-scale surveys of practice have demonstrated trends in the use of particular valuation techniques, and advances in real-options modelling have identified ways in which valuation practices might be modified and extended. Despite such research, our understanding of investment appraisal processes is seriously inadequate, as scholars in accounting and finance have acknowledged. In particular, little is known of how organizations may seek to establish congruence between individual investment decisions made in many different sub-units, and articulations of overall organizational strategy. The ways in which investments can build organizational distinctiveness have scarcely been addressed. Also, the capital budgeting literature has remained impervious to the rise in network forms of organization, which may call for processes of

<sup>1</sup> This study was made possible by the support and cooperation of many employees of Intel Corporation. We are indebted particularly to Andy Bryant, Gerry Parker, and Mike Splinter for granting permission for the study, and to David Layzell for his support and encouragement throughout. We are grateful for comments received from participants in research colloquia at INSEAD, the London School of Economics and Political Science, Michigan State University, University College Dublin, the University of Manchester, the University of Southern California, and the University of Ulster at Jordanstown. We are grateful also for comments received from Christoph Drechsler, Ian Garrett, Sue Haka, Bob Kaplan, Joan Luft, Mike Newman, Brian Pentland, Mike Power, John Roberts, Geoff Sprinkle, Norman Strong, Lenos Trigeorgis, and Yanling Zhang. The financial support of the British Design Council, the Centre for Analysis of Risk and Regulation, and PriceWaterhouseCoopers is gratefully acknowledged.

investment coordination between legally separate entities and the pursuit of strategies at interorganizational levels. This chapter reports the results of a four-year longitudinal field study conducted at executive office levels in Intel Corporation. It seeks to remedy the neglect of firm-level empirical analyses of capital budgeting, and of the mechanisms used to coordinate investment decisions and associated expectations in a manner consistent with overall organizational strategy. More specifically, it examines whether managers at Intel systematically coordinate investments in a manner consistent with the theory of complementarities.

The importance of coordinating individual capital investment decisions to produce the benefits of complementarity relations has been examined in several recent studies. As Milgrom and Roberts (1995*a,b*) note, such relations arise when additional investment in any one component of a system increases the returns to additional investment in the others. They have argued that, where extensive complementarities are present, value-maximizing results may be achieved only by coordinated change in all the components of a system—such as novel marketing policies, products, production processes and manufacturing capabilities—and not by altering one of these elements in isolation from shifts in the others. Brennan and Trigeorgis (2000), among others, have sought to promote real-options analyses to enable a firm's managers to formally appraise the value of such inter-related investments. At the interfirm level, Dyer and Singh (1998) have sought to elaborate the ways in which a firm may secure 'relational rents' through the creation of complementary assets with other corporations.

However, as several authors have noted, the significance of complementarity relations may extend far beyond the direct realization of increased profits from a particular set of investments. The identification and production of such relations may be central to the enactment of wider organizational strategies, as Roberts (2004), Siggelkow (2001) and Whittington and Pettigrew (2003) have argued. On this view, the pursuit of comparative advantage involves forming cross-sectional and time-series relations between investments, over a long period of time. Investments in a firm's unique elements of intellectual property and skill are thus to be combined with one another, and with other, more generic types of resources. This allows the formation of systems of mutually reinforcing assets that are distinct, and that may be difficult for competitors to replicate.

Despite the formal modelling of complementarity relations, and theoretical and empirical studies of their significance in the formation of

corporate strategies (Siggelkow 2001), there remains an empirical deficit in the study of the actual capital budgeting and investment coordination practices that are used by firms (Jensen 1993; Graham and Harvey 2002). This is particularly so with respect to field-based research that looks intensively at the investment appraisal practices of a single firm using a wide variety of data. More specifically, despite intuition and casual observation, little is known about the mechanisms (other than competitive markets) through which the coordination of investments and related expectations is achieved within and among firms (Miller and O'Leary 1997). Also, little is known about how the coordination mechanisms used by firms relate overall organizational strategy to financial evaluation techniques, such as net present value (NPV), payback, and return on investment (ROI), that form the core of traditional capital budgeting practices. While Graham and Harvey's recent survey of capital budgeting (2001) polls a large set of firms, poses a broad range of questions concerning whether and when particular valuation techniques are used, and provides unique information on the financing policies of firms, issues of investment coordination are not addressed specifically. For instance, their questionnaire does not ask whether managers consider the scope of an investment decision, what mechanisms enable them to define this scope, and, if there are complementarities to be economized upon, what practices are used to coordinate investments within and among firms and to value the set of synergistic assets.

To analyse the implications of interfirm and intrafirm investment coordination for overall organizational strategy, we focus on a hitherto neglected mechanism—the technology roadmap—which is an important part of Intel's capital budgeting process. While the existence of roadmapping practices has been noted in the literature outside accounting, their role in investment appraisal has not been explored to date. Technology roadmaps are used to ensure that large-scale capital investments made by sub-units of the firm (in assets such as new processes, microprocessor products, and manufacturing capacity) are coordinated with one another, and that they are aligned, also, with investments in enabling and related technologies on the part of a wide range of other firms, including those in Intel's supplier base, its OEM customers, and developers of operating systems, software, and communication infrastructures. We describe the technology roadmap mechanism, and we examine how it integrates with discounted cash flow (DCF) analyses to permit an individual capital spending proposal, such as in a new microprocessor product, to be valued within the system of complementary investments of which it is a part. We examine also the role

of industry-level technology roadmaps produced by the Semiconductor Manufacturing Technology (SEMATECH) consortium, and how these support firm-level coordination of investments and related expectations.

There has been some prior attention to the technology roadmap mechanism in the practitioner literature. Willyard and McClees (1989) have offered a short and purely descriptive treatment of its use within individual business units of Motorola. Spencer and Seidel (1995) have recounted the early stages of adoption of roadmap practices by the SEMATECH consortium, drawing on the first author's recollections as CEO of that body. In academic literature, Browning and Shetler's history (2000) of SEMATECH notes briefly how roadmap practices helped the consortium to supplant its early (and controversial) role as builder of globally competitive US firms with the seemingly more neutral one of aligning technology development plans. This chapter differs from the existing literature on roadmap practices in providing a detailed empirical analysis of how they enable the coordination of capital spending decisions at intra- and interfirm levels, and how this is relevant for accounting research.

The chapter contributes to research on managerial accounting, capital budgeting, and strategy in two key respects. First, and in contrast to existing studies that operate only at the intrafirm level (Miller and O'Leary 1997), it provides a detailed description and analysis of a set of practices that are largely unreported within the accounting literature. It examines the roles of technology roadmap practices in aligning capital spending decisions across sub-units of the firm and across firms. Particular attention is paid to how roadmap practices enable such decisions to be coordinated on a dynamic basis, thus facilitating the 'active management' of investment programmes that has become a key concern in recent theoretical and normative literatures on the capital budgeting process (Trigeorgis 1996; Brennan and Trigeorgis 2000).

Second, there is a contribution to the literature on the design of accounting control systems, and strategy at the interfirm level. What Doz (1996) terms 'initial complementarity', the prospect of synergies from interfirm investment coordination, may fail to give rise to actual or 'revealed complementarities' because the resources in a network of firms co-evolve in ways that 'lock [individual partners] into unproductive relationships or preclude partnering with other viable firms' (Gulati et al. 2000). Calling for research to examine 'the factors that impede the realization of relational rents' at the interfirm level, Dyer and Singh (1998) suggest, as a starting point, that each firm should consider the

potential for loss of flexibility at the time a network is formed. Our analysis of technology roadmapping practices shows how the problem of lock-in may also be addressed at an earlier stage in the technology development process. In particular, we demonstrate how the roadmap provides a mechanism for stimulating and monitoring competition in component and technology development before specific networks are formed. Such a mechanism complements the kinds of 'interfirm design instruments' or control systems that are more usually studied and that focus on organizational and information-sharing arrangements as partners enact a particular long-term alliance (Baiman and Rajan 2002).

The remainder of the chapter is organized as follows. Section 2 describes our field research methods. Section 3 analyses the structure of the complementarity relations available to Intel. Section 4 examines the roles of technology roadmaps in coordinating investments at inter- and intrafirm levels. Section 5 provides implications for future research and conclusions.

## Method

Permission to undertake research within Intel was sought initially in negotiations with an executive vice-president of the firm. Approval was granted subject to signing a formal non-disclosure agreement. This allowed the researchers to gain access to private information, and to study the application of the firm's investment coordination and appraisal practices to a particular technology generation during the period May 1996 to June 2000. Release from the non-disclosure agreement was secured at the conclusion of the research, so that the firm's identity could be revealed. This process did not constrain the arguments and evidence presented in this chapter, and Intel did not require any particular items of data, analysis, or argument to be included in the manuscript or excised from it.

By negotiating access to the most senior managerial levels of Intel, and conducting a multi-year study, it was possible to identify sources of data and to examine materials relating to the firm's actual capital budgeting process that are inaccessible to survey-based and large sample studies (Graham and Harvey 2001). Such a detailed and extensive piece of field research is unusual in the literature. However, any such study has the inherent limits of a small sample, with the inevitable constraint that its results may be sample specific. This may be overcome in

subsequent research, in particular by utilizing the detailed empirical description provided for theory development and communication.

Four research methods were used to compile a substantive database. These were interviews with key decision-makers, the manual collection and analysis of internal documents, first-hand observation of processes, and the collection and analysis of the public record concerning the firm and the industry.

Given the concern to study the coordination of major capital investments, interviews were sought with many of the firm's most senior officers. Interviews were requested with thirty-three executives and managers, selected for their roles in making investment decisions and in developing and extending the firm's capital budgeting practices. All of those approached agreed to be interviewed. All interviews were conducted by the authors. Most of these were at Intel's corporate offices in Santa Clara (California), and at its facilities in Chandler (Arizona), Albuquerque (New Mexico), and Hillsboro (Oregon), and the remaining were at one of the firm's manufacturing facilities in Leixlip (Ireland). Those interviewed included: the president and CEO; the chief financial officer; vice-presidents for technology development, manufacturing, microprocessor product design, and marketing; the director of technology strategy; and managers and engineers in R&D facilities and high-volume factories. In addition, interviews were conducted with three technical analysts who focus exclusively on examining the semiconductor industry for the primary trade publications. They were asked to describe their understanding of Intel's coordination practices. All interviews were semi-structured and lasted a minimum of one hour. All but three of the interviews were tape-recorded.

The researchers gained access to and analysed a range of documents confidential to Intel. These included the firm's capital investment manual, engineering and technical manuals, and the proceedings of intra-firm conferences that describe how investment appraisal and coordination practices were devised and how they have been modified and extended in use. Intel fabrication facilities in Ocotillo (Arizona), Rio Rancho (New Mexico), and Leixlip (Ireland) were visited, to gain a first-hand understanding of the firm's technology development and manufacturing processes.

Internal data sources were complemented by analyses of the public record concerning the firm and the industry. Press releases and press coverage were studied, as well as speeches by Intel executives, the proceedings of trade conferences, technical and trade journals, and the reports of technical and financial analysts.

## The firm and its complementarity structure

Intel designs and manufactures microprocessors, the logic devices that enable computers to execute instructions.<sup>2</sup> Throughout the 1990s, its share of the worldwide market for PC microprocessors exceeded 70 per cent of units shipped. During the same period, the firm's ratios of gross profit and operating profit to net revenues generally exceeded 50 per cent and 30 per cent, respectively. The ratio of operating profit to total assets generally exceeded 20 per cent, such that key analysts ranked Intel the world's most profitable microprocessor producer.<sup>3</sup> A key element in the firm's strategy has been to invest, at frequent intervals and in a coordinated manner, in improved fabrication processes, new products, and enhanced manufacturing practices.

Since the mid-1980s, Intel has invested in an improved process for fabricating microprocessors, termed process generation, at intervals of approximately three years. In addition, and at comparable intervals, it has designed at least one new family of microprocessor products, and commenced manufacture in three to six geographically dispersed factories, each of them incorporating improvements in layout, operating policies, training, and other procedures. This process of recurrent investment in both products and processes requires substantial levels of intra- and interfirm coordination. Developers of Intel's proprietary process generations collaborate closely with a range of suppliers such as Silicon Valley Group and Nikon that are investing concurrently to design more advanced equipment sets and materials. Without corresponding advances in lithographic equipment sets manufactured by those firms occurring at defined moments, Intel would be unable to operationalize its successive generations of process technologies. The value of advances in microprocessor design would thus be substantially reduced. Also, Intel's microprocessor architects seek to coordinate their designs with those of customers and firms that are investing in complementary products. These include computing devices by Dell, Compaq, Fujitsu, and others, operating systems by developers such as Microsoft and Linux, database management systems, and extensive sets of application software programmes. Again, without these complementary investments being made by other firms, and their timing being carefully and

<sup>2</sup> The firm also manufactures hardware and software products for Internet-based and local-area networking, as well as chip-sets, motherboards, flash-memories, and other 'building blocks' for computing and Internet-based communication.

<sup>3</sup> M. Slater, 'Profits Elude Intel's Competitors', *Microprocessor Report*, 10 May 1999.

accurately synchronized, the financial gain to Intel of improvements in the speed of microprocessors arising from process and product advances would be substantially less.

Through the coordination of investments within the firm, and with both upstream and downstream firms, Intel's executives seek to economize on what Milgrom and Roberts (1995*b*) have termed a 'complementarity structure'. In this section, we set out the components of this complementarity structure, as a prelude to examining in Section 4 the mechanisms that are used to coordinate them. In the three subsections that follow, we examine the separate sets of relations comprising that structure. First, we examine how they may arise when a new process generation is developed and operationalized concurrently with new microprocessor products. Second, we look at the benefits available when new microprocessor product designs align with complementary computing, operating system, and software products. Third, we consider how complements may be achieved when a new process generation is accompanied by advances in the designs of Intel's high-volume factories. To illustrate the importance of successful coordination, and how critical timing is, the fourth and final subsection illustrates the costs to the firm of failing to align successfully the overall set of complementary assets.

### **Coordinated process generation and microprocessor designs**

The aim of investing in each new process generation is to reduce the minimum linear feature size of an electronic element, such as a transistor, so that more of them can be formed on a silicon wafer.<sup>4</sup> This increase in transistor density has two main effects. First, it increases the yield of good microprocessor die per silicon wafer (die-yield). Second, it improves the speed at which a microprocessor can execute instructions (clock-speed).<sup>5</sup>

Intel's executives seek to establish and optimize complementarity relations by coordinating incremental investments in a process generation that increases transistor density, and incremental investments in

<sup>4</sup> At present, electronic elements below 0.09 micron in length are being patterned on wafers and, historically, the length has been reducing by a factor of  $\sim 0.7$  per process generation. A micron equals 1/1,000,000 of a metre.

<sup>5</sup> As feature-sizes are reduced, electrons take less time to complete an electronic circuit, thus enhancing the clock-speed of the microprocessor.

new products. The design of a new product generally consists of extensions to an architecture, so that the microprocessor can execute an enhanced set of functions at a faster clock-speed. A typical effect is to increase the number of electronic elements on the microprocessor die, thus increasing its area and reducing die-yield per wafer on a given fabrication process (see Appendix). The returns to coordinated introduction of a new process generation and a new microprocessor are generally higher than to both changes made independently. The increased transistor density of the process at least partially offsets the larger die-size of the product, resulting in lower unit costs of manufacture. It also boosts the clock-speed increases that are achieved by improvements to the product architecture. The coordination of investment in process generation and microprocessor design forms the initial step in the production of complementarity relations. A second step is to seek to align the designs of the microprocessor products with those of complementary products.

### **Coordinated microprocessor and complementary product designs**

Intel's strategy is to lead competitors in introducing new microprocessor products, and to coordinate the launch of each one with the introduction of more advanced computing devices, operating systems, and application software designed by other firms. To achieve this, timing is critical. An executive board member and president of Intel Capital commented that his main concern was to achieve two things: first, to ensure 'that our strategies are aligned with our complementors', and second, to speed up the programmes of complementors if necessary to make sure that 'when their product gets to the market, it is pretty much in-time with our product, not a year or two years later...'<sup>6</sup> The benefit to Intel in both cases is to increase the speed at which high volumes can be achieved with a new generation of technology. With a market share in excess of 70 per cent, the firm's revenue growth rate was seen to depend increasingly upon the formation and expansion of markets rather than an increase in market share. As the manager responsible for Technical Analyst Relations commented: 'We started moving into a mentality that went along the lines: if we can do things that stimulate the market

<sup>6</sup> Interview, executive board member and president of Intel Capital, 28 July 1998.

growth, we will assume that we are going to take our fair share of that position.'<sup>7</sup>

From its dominant position within the microprocessor market, Intel aims to produce complementarities that are available through coordinating investments at the interfirm level. The timing of the launch of a new microprocessor is critical, since Intel usually introduces a new microprocessor at a relatively high price, which is then reduced significantly during the product's short life cycle. The aim is to secure product acceptance on the part of the most demanding users initially, while the product is still manufactured in low volumes in the development factory, and then to stimulate demand growth by lowering prices as additional factories are brought on-stream. Life cycle revenue is thus significantly higher for Intel when its product investments are coordinated successfully and precisely with those of related firms, such that a new microprocessor, enhanced operating systems, improved Internet infrastructures, and novel software applications are all available from the outset of a given generation.

### **Coordinated process generation and factory designs**

The third element in the complementarity structure involves the coordination of investment in each process generation with investment to enhance Intel's high-volume manufacturing capabilities.

While successive process generations offer increases in die-yield and clock-speed, each one also involves working to finer tolerances, across a greater number of manufacturing steps, using several equipment types and materials that are new to the firm and to the industry. Performance levels achieved in the development factory become more difficult to sustain as successive process generations are transferred to high-volume manufacturing facilities, whose personnel have to learn the parameters of increasingly complex systems. Lower performance levels during the learning period could require investment in excess capacity to achieve a given level of output, thus diminishing the benefits Intel gains from stimulating high-priced, early-period demand for new microprocessors.<sup>8</sup>

<sup>7</sup> Interview, Manager, Technical Analyst Relations, 24 August 1998.

<sup>8</sup> Interview, Director of Technology Strategy, 11 December 1996.

The firm seeks complementarities by coordinating the introduction of each process generation, offering enhanced die-yields and clock-speeds, with advances in factory design aimed at reducing the time to learn new system parameters. Since the early 1990s, and to combat the so-called 'Intel-U',<sup>9</sup> the firm has sought closer integration of its development site and high-volume factories, using 'virtual factory' control practices. The intent has been to engineer each generation of high-volume factories so that it more closely copies and reflects the exact layouts, equipment sets, operating procedures, and intervention policies established in the development site. The trajectory of improved performance in the development site is thus to be continued within each of the high-volume factories, as though the network as a whole comprised a single manufacturing entity.

### **Costs of a coordination failure**

There are costs of coordinating investments in process, product, and factory designs with one another internally, and with those of suppliers, complementors, and customers externally. They include the expense of the organization structures and systems by which various groups align their design decisions. Also, there are costs of rendering product development resources fungible, so that, for instance, groups of architects may be re-assigned to develop a particular microprocessor more quickly to synchronize with the earlier availability of a process generation. Historically, Intel executives have found such expense to be substantially lower than the benefits. As the Chief Financial Officer remarked: 'We will take a new process [generation] as soon as we can get one, and we will put as many products on the new process as we can, and incur any [incremental] cost necessary.'<sup>10</sup> The returns from a new process are considered to be so great that the limiting factor is regarded as technological rather than financial.

Table 5 estimates the manufacturing costs of one hypothetical coordination failure, in which the 0.25-micron process generation becomes

<sup>9</sup> The phrase is part of Intel folklore. It refers to the early history of process transfers, when product yield would decline significantly each time a process generation was transferred from development to high-volume factories, and would remain depressed for several months, resulting in a U-shaped yield curve.

<sup>10</sup> Interview, Chief Financial Officer, Intel Corporation, 26 August 1998.

available one quarter later than the Pentium II microprocessor product. It is assumed that volume of sales for the quarter remains unchanged, but in the absence of newer fabrication technology Pentium II would continue to be manufactured on the earlier 0.35-micron process generation. As a consequence, the product's die-size is larger and the yield of good die is lower. Each wafer produces only 58 good dies, compared with 120 if the newer fabrication process were available. The net effect of the delay is excess manufacturing cost of \$480 million, almost 6 per cent of Intel's operating income for the year 1998. Even relatively short lags between the arrival of a fabrication process and a product may thus result in significant diminution in Intel's operating income.

**Table 5** Estimated manufacturing cost of a failure to coordinate process generation and product designs

<b>Condition</b>	<b>Process lags product by three months</b>	<b>Synchronized designs</b>
<b>Process Generation (micron)</b>	0.35	0.25
<b>Product</b>	Pentium II	Pentium II
<b>Die-size and yield data</b>		
Microprocessor die-size (mm <sup>2</sup> )	203	131
Yield of good die per silicon wafer	58	120
<b>Estimated manufacturing costs per good die (\$)</b>		
Fabrication	49	28
Package	16	16
Packaging and testing	15	12
Module parts and assembly	14	14
Total manufacturing cost per good die (\$)	94	70
<b>Manufacturing cost of coordination failure</b>		
Unit cost difference (\$94 – \$70)	24	
Volume (first quarter, 1998 estimated unit shipments of Pentium II)	20 million	
Estimated total cost of coordination failure (\$)	480 million	
Excess cost as % (1998) operating income (\$8,379,000,000)	5.7	

*Note:* Intel Corp., Microprocessor Reference Guide (2000) and press releases; L. Gwennap and M. Thomsen, *Intel Microprocessor Forecast* (Sebastopol, CA: Micro Design Resources, 1998).

In the following section, we analyse how Intel seeks to avoid such costs, and to realize the benefits available from the complementarity structure, through practices of intra- and interfirm investment coordination.

## Technology roadmaps

Consistent with the large-scale firms surveyed by Graham and Harvey (2001), Intel's capital budgeting process requires discounted cash flow (DCF) analyses. Net present values (NPVs) are calculated for proposed new microprocessors within the product development groups, for instance.<sup>11</sup> Net present cost analyses are used extensively, as when factory planners are choosing between capacity installation alternatives, such as whether to refit an existing facility for a new process generation or build from a greenfield site, or whether to expand production in one country rather than another.<sup>12</sup>

In light of the extensive set of complementarities available to the firm, however, the capital budgeting process restricts the right of sub-units to evaluate investments 'independently at each of several margins', in Milgrom and Roberts' phrase (1990: 513). To be approved, an investment proposal must not only promise a positive return, but also align with a technology roadmap.<sup>13</sup>

A technology roadmap sets out the shared expectations of the various groups that invest to design components, as to when these will be available, and how they will interoperate technically and economically, to achieve system-wide innovation. Typically, it will address each of several future coordination points, defined by a year or quarter-year. The groups involved in preparing it may include sub-units of a firm, as well as suppliers, complementors, and OEM customers. A roadmap is an inherently tentative and revisable agreement, one of whose key roles is to enable design groups to assess the system-level implications of advances, delays, or difficulties in bringing investments in new component

<sup>11</sup> Interview, Vice-President, Microprocessor Products Group, 25 July 1996.

<sup>12</sup> Interview, Chief Financial Officer, Intel Corporation, 26 August 1998. Net present cost analyses establish discounted cost differentials, taking revenue to be the same across alternatives.

<sup>13</sup> Intel Corporate Finance, *Capital Project Authorization* (1998) (internal document); Interview, Corporate Capital Controller, 23 July 1996.

designs to fruition.<sup>14</sup> Equally, the expectations reflected in a technology roadmap may require fundamental revision if there are indications of insufficient demand for the end-user products to which the system of component innovations is expected to give rise. A roadmap thus provides a mechanism for the dynamic coordination of expectations where there is recurrent intra- and interfirm investment.

Through linking an investment explicitly with a technology roadmap, the proponent is required to demonstrate that it synchronizes and fits with related and complementary investments within and beyond the firm. Ensuring that individual investment decisions are congruent with the relevant roadmap is afforded the highest priority by Intel's executive officers. The complementarity structure is considered to be of such importance that it is addressed directly by the president and CEO. As he remarked: 'We obviously do ROIs on products and things of that sort, but the core decisions the company makes, the core decisions are basically technology roadmap decisions...'<sup>15</sup>

In the subsections that follow, we analyse and illustrate how a technology roadmap is prepared and the roles it plays in investment coordination. We follow the chronology of roadmap preparation, beginning with the alignment of investment decisions between Intel and firms in its supplier base.

### **Coordination with suppliers' innovations**

Intel depends upon innovations by suppliers of equipment sets and materials to operationalize each of its new process generations, and thus begin its cycles of complementary investment in process, product, and factory designs. The firm regards such innovations on the part of

<sup>14</sup> However, the costs of revision to individual sub-units and firms may increase as a particular coordination node approaches, because each will have invested in the expectation of system-wide success.

<sup>15</sup> Interview, President and CEO, Intel Corporation, 17 December 1998. By 'ROIs', the CEO means summary financial statistics, including NPV and net present cost, as mandated by Intel's Capital Project Authorization manual. 'Moore's law' is named for Intel co-founder and chairman-emeritus Gordon Moore, who noted in 1975, and on the basis of empirical observations extending across fifteen years, that the semiconductor industry seemed capable of doubling the number of electronic elements on a memory device every eighteen months. See Moore (1975).

suppliers as benefiting the industry as a whole, and cooperates with other semiconductor manufacturers to specify collective design needs and time-lines. As the president and CEO of Intel remarked, it is 'much more economical for our industry to work as a whole to create some base technology, and the real intellectual property, the real value-added, comes not from creating a stand-alone piece of lithographic equipment, or a stand-alone piece of ion implanter [equipment]; it comes from the integration of those into a total process'.<sup>16</sup> This means that Intel is able to work with competitors in creating stand-alone pieces of technology, while seeking to gain a competitive advantage from the integration of the different components.

Coordination of investments by semiconductor firms and their supplier base is facilitated by a technology roadmap that is prepared under the auspices of the SEMATECH consortium. Table 6 shows top-level statistics from such a roadmap that was published in 1994. It was prepared by delegates from each of the thirteen firms comprising the consortium, including Intel, which accounted collectively for over 80 per cent of the US output of semiconductor devices. They collaborated with trade associations representing supplier firms through joint working groups and conferences, and liaised also with relevant US federal and university laboratories. The resultant roadmap indicated the design requirements for equipment sets and materials at each of five future coordination points.

The preparation of the technology roadmap may be divided for analytical purposes into three steps. The first step was to specify rates and directions of change in individual design variables to achieve coordinated results at each point or node (Table 6). The intention was to indicate to suppliers when the US semiconductor industry would demand novel equipment sets and materials of particular tolerances and capabilities, in sufficient quantities for high-volume manufacture. The changes in design variables were specified by extrapolation from historical performance levels, specifically, by assuming that the innovative conditions under which Moore's law had been achieved in the past could be made to persist. As the Manager of Lithography Process Equipment Development commented, while Moore's law is not a law of physics, 'it's a pretty strong economic law because once the industry deviates from Moore's law, then the rate of investment is going to

<sup>16</sup> Interview, President and CEO, Intel Corporation, 17 December 1998.

**Table 6** Required rates and directions of change in individual design variables to achieve coordinated and system-wide innovation as specified in National Technology Roadmap for Semiconductors (1994)

Technology node	Current			Future		
	( $N_0$ ) 1995	( $N_1$ ) 1998	( $N_2$ ) 2001	( $N_3$ ) 2004	( $N_4$ ) 2007	( $N_5$ ) 2010
<b>Suppliers' innovations in equipment sets and materials<sup>a</sup></b>						
Lithography						
Minimum feature size ( $\mu\text{m}$ )	0.35	0.25	0.18	0.13	0.10	0.07
Scaling factor per generation		$\sim 0.7$				
Silicon wafers						
Wafer diameter (mm)	200	200	300	300	400	400
Increase per two generations (mm)			100		100	
<b>Advances in semiconductor product designs</b>						
Memories						
Bits per die (millions)	64	256	1,000	4,000	16,000	64,000
Multiple per generation		4	$\sim 4$	4	4	4
Cost/bit (thousands of a cent)	0.017	0.007	0.003	0.001	0.0005	0.0002
<i>Scaling/reduction factor</i>		$\sim 0.45$	0.5	$\sim 0.5$	0.5	$\sim 0.5$
Microprocessors						
Transistors per die (millions)	12	28	64	150	350	800
Multiple		$\sim 2.3$				
Cost/transistor (thousands of a cent)	1	0.5	0.2	0.1	0.05	0.02
Scaling/reduction factor		0.5	$\sim 0.5$	0.5	0.5	$\sim 0.5$

<sup>a</sup>For brevity of exposition, only two types of components whose designs are coordinated are included here; the full version of the roadmap includes many others, such as deposition and implantation equipment, mask technologies, etc.

Note: Adapted from Semiconductor Industry Association, *National Technology Roadmap for Semiconductors* (San Jose, CA: SIA, 1994: B-2).

change, and the whole structure will change...'.<sup>17</sup> Were that to happen, it would indicate that the industry as a whole was maturing.

It was anticipated that electronic feature sizes could continue to be reduced at a rate of 0.7 per coordination point due to investments in innovation by lithography suppliers, and that this would combine with certain minimum rates of increase in wafer diameter achieved by silicon suppliers (Table 6). Coordinated availability of these and other newly developed components would permit semiconductor firms to continue to operationalize new process generations that would increase the number of bits on a memory product by a factor of four,<sup>18</sup> and the number of transistors on a microprocessor die by a multiple of ~2.3. While the roadmap thus indicated when the US semiconductor industry expected to demand components of given capability, it deliberately avoided 'specifying preferred technology solutions or specific agendas that particular organizations should follow'.<sup>19</sup> The intention was that suppliers should compete to establish the most effective technologies for meeting demand at various coordination nodes.

The second step was to provide an intensive, industry-wide assessment of the state of component R&D, so as to focus the attention and the investments of suppliers on the most promising technology alternatives. In the case of the later coordination points particularly, a number of alternative technologies were identified in each of several critical areas that might meet the industry's requirements if further researched and developed. The aim in clearly identifying them was to bring about a form of coordinated competition on the part of suppliers, so that they would concentrate investment on the commercialization of alternatives regarded as most likely to succeed for a given coordination node by the consensus of industry experts.

For the case of lithographic equipment, the roadmap identified three potential technologies—proximity X-ray, e-beam projection, and extreme ultraviolet (EUV)—for patterning electronic features of 0.1-micron and below. Each of them had proponents among semiconductor firms and within the supply base. IBM and others contended that X-ray machines would be superior, and invested accordingly, whereas Lucent

<sup>17</sup> Interview, Manager of Lithography Process Equipment Development, 3 November 1997.

<sup>18</sup> This is the rate of increase in electronic elements on a memory device that Moore's law calls for, viz. a multiple of four per three years, or two per eighteen months (Moore 1975). The industry established a different constant for increases in microprocessor functionality, viz. a rise in the number of transistors per die by a multiple of ~2.3 every three years.

<sup>19</sup> Semiconductor Industry Association, *National Technology Roadmap for Semiconductors* (San Jose, CA: SIA, 1994: 1).

expended significant R&D on e-beam projection. Other suppliers, supported by Intel, proposed development of EUV machines.<sup>20</sup> The roadmap anticipated that semiconductor firms would select only one of the technologies for use in high-volume production, thus enabling them to share the high costs of R&D. The successful technology could thus enjoy industry-wide demand for several coordination nodes.

During 1997, Intel formed a private industry consortium with two other semiconductor firms, AMD and Motorola, to accelerate the development of EUV lithography. The consortium invested \$250 million of venture capital in EUV projects at three US Department of Defence laboratories. The intent was to leverage the R&D programmes of suppliers committed to EUV. They could delay substantial investment in its commercialization until the laboratories, which had pioneered the early stages of EUV technology, had pilot-tested its ability to pattern electronic features reliably. Equally, the consortium's approach enabled Intel, AMD, and Motorola to delay lock-in to a long-term design and supply relationship with the EUV suppliers, until after 'proof of concept' had been established. The manager of Technical Analyst Relations commented, with respect to the three different forms of advanced lithography under consideration at the time, '[W]e think the industry will only support one of these three, and Intel has said, up front, if somebody else comes up with a better idea, we are not going to be proud, we are going to adopt it. We'll go whichever way.'<sup>21</sup> So, while Intel might invest in one particular technology, it will also observe closely developments in other substitute and competitor technologies, and make prototype machines available on the open market so as to encourage competition.

The third and final step in the SEMATECH roadmapping process was for the consortium to agree to revisit the feasibility of projections in a series of frequent update meetings. These may consider arguments from members to alter conditions such as the frequency with which the industry will shift to novel sets of technologies. During 1994, for instance, Intel executives concluded that two-year innovation cycles were more likely to be optimal for the firm than the historical three-year cycle. The decision was based on a DCF analysis of whether more frequent increments in transistor density and microprocessor clock-speed, available from two-year cycles, would outweigh such costs as faster obsolescence of process generations and products.<sup>22</sup> In extensive negotiations with consortium

<sup>20</sup> C. Fasca, 'Litho Powerhouse Formed', *Electronic News*, 15 September 1997.

<sup>21</sup> Interview, Manager of Technical Analyst Relations, 24 August 1998.

<sup>22</sup> Interview, Chief Financial Officer, Intel Corporation, 26 August 1998.

members and the supply industry, a temporary shift to two-year cycles was agreed with respect to the 0.25-, 0.18-, and 0.13-micron nodes, with a reversion to three-year cycles thereafter (Table 6).<sup>23</sup> Also, the revision meetings are used to monitor whether the development of alternative component technologies is proceeding as anticipated. In the case of lithography, SEMATECH members concluded during the late 1990s that enhancements to an established technology—deep ultraviolet—would serve the industry for patterning feature sizes of 0.1-micron and smaller. As a consequence, investments in the commercialization of X-ray, e-beam, and EUV technologies were further deferred.

The SEMATECH technology roadmap thus provides a mechanism for coordinating expectations and investments among a set of firms and its supplier base in a key sector of the modern economy where there is recurrent and system-wide innovation. In addressing design requirements comprehensively for all core types of components, it reflects the dependence of investment returns to any one specialized firm on close coordination with the design plans of others. All the technology elements need to be in place before a transition can be achieved to the next generation.<sup>24</sup>

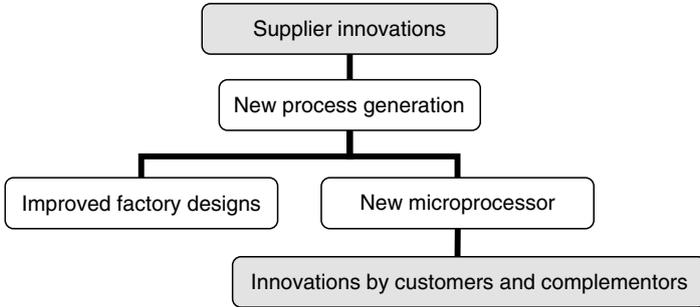
Partial coordination of a system of investments may not come close to producing optimal returns in this industry, an observation consistent with the implication that Milgrom and Roberts (1995*b*) derive from their models of complementarity relations. By establishing where design lags are most likely to occur at each of several future nodes, and then identifying and monitoring promising alternative lines of technology development, the roadmap may enable firms to avoid premature commitment to any one particular technology and set of interfirm relations. And by affording opportunity to lobby for changes in the roadmap, the SEMATECH process acknowledges the inherently high levels of uncertainty affecting all parties, and the need to focus attention and resources on any unexpected technical and financial difficulties affecting particular firms or sectors.

### **Intrafirm coordination**

In light of the shared expectations formed with suppliers, Intel managers continue the roadmap preparation procedure inside the firm. They plan

<sup>23</sup> A revised version of the SEMATECH roadmap incorporating the changes was published during 1997.

<sup>24</sup> Semiconductor Industry Association, *National Technology Roadmap for Semiconductors* (San Jose, CA: SIA, 1994: 27).



**Figure 12** Components of the 0.25-micron technology generation whose design Intel sought to coordinate at intra- and interfirm levels. Components developed by other firms are indicated by shaded boxes.

several future process generations to coincide with the availability of more advanced equipment sets and materials. Three primary pieces of data are recorded in the intrafirm roadmap with respect to each generation: when it is expected to be available for test production and high-volume manufacture; the key technical changes it is to introduce, particularly with respect to additional transistor density; and the expected capital investment to install a unit of capacity utilizing the new process.<sup>25</sup> The data are communicated to Intel's factory design group and microprocessor architects, so that they may extend the intrafirm roadmap to show the combined financial effects of aligning the introduction of each process generation with that of more advanced manufacturing practices and new products.

In 1994, for instance, the intrafirm roadmap showed the planned availability during 1997 of a process generation to pattern 0.25-micron transistors on silicon wafers (Figure 12). To partially offset the rise in investment per unit of capacity associated with the more advanced process, factory designers sought to coordinate its introduction with that of improved manufacturing layouts and operating policies in high-volume factories:

I am designing policies hand-in-hand with the people who are currently developing [a process generation]. So it is meant to be a continuum. . . . [We] design a continuum of policies, so that we have a set of policies that's intended to maximize information turns in a technology development factory, and in early

<sup>25</sup> A unit of capacity is measured as a given number of wafers introduced into production in a week (e.g. 5,000 wafer-starts-per-week). Capital investment data are only communicated selectively within the firm, to senior managers who require it as input to their investment proposals.

high-volume factory to maximize output, late high-volume to minimize cost, ramping to maximize the ramp velocity. We need—in a factory, at a given snapshot in time—a WIP policy, an equipment maintenance policy, a cross training policy, etc., etc., that fit together.<sup>26</sup>

Of particular concern was the need to increase ramp-velocity by altering factory layouts and equipment installation, staffing, and operating policies. Ramp-velocity is a measure of how quickly a new process generation can be ‘copied’ from its development site to high-volume factories without impairing a given level of die-yield. The faster this is achieved, the lower the total investment needed to meet a given volume of demand, and the greater the financial benefits of a new process generation.

Microprocessor architects extended the intrafirm roadmap still further, by planning the investment schedules and time-lines of several new product families to coincide with the availability of the new process. By examining this alignment, we demonstrate the roles of a technology roadmap in permitting capital spending on new products to be appraised within the system of complementary assets of which they are to form a part.

Capital spending on a new microprocessor is typically proposed in stages, during a period of four or more years. Early investment is aimed at deriving a general model of the enhanced capabilities the new product might deliver for particular market segments, without commitment to a precise time-frame for execution or to manufacture on a given process generation. But, as architects move from that model to instantiating the new product as a set of circuits, layouts, and masks necessary for manufacture, returns to additional investment come to depend significantly on coordinating product design closely with that of a particular process generation. The investments needed to achieve this are substantial. As the vice-president of the Microprocessor Products Group commented, ‘I may spend in the order of a hundred-engineer-years of creating a physical layout only to find that I have to re-do it for the next generation [process] technology.’<sup>27</sup>

A technology roadmap provides a mechanism for appraising whether such irreversible investment is justifiable in light of the investment time-lines and expected capabilities of complementary components. During the early 1990s, for instance, Intel executives decided that, in addition to designing further products within its 32-bit architecture, the

<sup>26</sup> Interview, Principal Scientist, Manufacturing Systems, 22 August 1997.

<sup>27</sup> Interview, Vice-President, Microprocessor Products Group, 25 July 1996.

firm would also develop a line of new 64-bit microprocessors aimed at higher-end workstation and server markets. A processor code-named Merced, devised jointly by Intel and H-P, was planned as the first instantiation of the new architecture. By consulting the technology roadmap, product architects sought to align their investment in the new product with the availability of a suitable new process generation:

[The technology development] organisation is very good at putting out a roadmap internally as to when they expect a certain process generation to arrive. It is based on history of how often we have been able to increment the process generations, and based on a forecast by some people in [the] organisation that are continually looking at where they expect, for example, lithography to evolve [by] a certain point of time. So, the [product] design group and myself, or general manager at the time, would have access to this technology roadmap . . . that says, basically, as a function of time, this is the beginning point of the ramp of the .35-micron generation, for example, this is the entry point of the .25-micron generation, this is the entry point of the next generation that will follow that. . . . The decision [on coordinating] a high-end product like this Merced [with a particular process generation] . . . is actually very easy, in the sense that your product is oriented for performance. There is only one promise that you have [for customers] on this product, and that is that you'll offer the highest performance capability at the time for these high-end systems. So, you want to implement that on the most advanced [process] technology that would be available for manufacturing at the time the product would come out.<sup>28</sup>

The initial decision of the product architects was that the Merced should be introduced during the life cycle of the 0.25-micron process generation during 1998 or early 1999 (Figure 12). They believed that the product time-line could be made to align with that of the process, that the size of the product would permit an acceptable die-yield per wafer using transistors of 0.25-micron in length, and, generally, that an acceptable NPV would result from such a coordination.

The decision to launch a powerful and large die-sized product such as the Merced on the 0.25-micron process was based on a key assumption that the product would quickly be shifted to the newer 0.18-micron process generation. Not only was that generation expected to offer a further increase in transistor density, it was also anticipated that it would operate on larger, 300-mm silicon wafers, which were in the course of being developed by suppliers. As a consequence, the relatively large die-size of a product such as Merced would quickly be offset by process generation advances, such that an acceptable long-run yield of

<sup>28</sup> Interview, Vice-President, Microprocessor Products Group, 25 July 1996.

good die per wafer could be achieved. However, unexpected revisions to the process roadmap in October 1997 led to a fundamental revision of such expectations.<sup>29</sup>

The expectation that suppliers could develop and supply the larger wafers in time for the 0.18-micron generation had proven to be incorrect. In addition, as Merced's designers sought to perfect the new 64-bit architecture, they found during 1997 that the die-size of the product would be significantly larger than had been anticipated.<sup>30</sup> A key role of the technology roadmap mechanism is to convey such shifts in expectations, which may arise inside or outside the firm, to product developers to inform their capital investment decisions. Influenced by the delay in arrival of the larger wafer size, and also by difficulties in perfecting the Merced's instruction set, Intel's executive officers decided during 1997 to defer its launch, and the product's development time-line was reset so as to coincide with a later process generation.

However, the time-line and technical attributes of the 0.25-micron process were found to be fully aligned with those for a second family of new microprocessors, the Pentium II. As the general manager responsible commented: 'Pentium II was clearly the flagship product of our 0.25-micron technology. I want to make sure that the 0.25-micron technology is well suited for this product.'<sup>31</sup> This involved close collaboration between process engineers and product architects so that, as the Pentium II instruction set was refined and as its circuits and layouts were completed during 1996 and 1997, the emerging 0.25-micron process generation was adjusted to support features critical to its performance. Intel personnel thus sought to maximize the clock-speed of the new product while keeping its die-size sufficiently small for economic manufacture. The Pentium II contained 7.5 million transistors, 36 per cent more than its direct predecessor, the Pentium Pro. But coordination of decisions on the part of product architects and process engineers resulted in a die-size for the new product that was actually 33 per cent smaller than that of the Pentium Pro (Table 7). Also, whereas architec-

<sup>29</sup> Interview, Manager of Lithography Process Equipment Development, 3 November 1997.

<sup>30</sup> Interview, Chief Financial Officer, Intel Corporation, 26 August 1998; L. Gwennap. Intel's Two-Track Strategy Re-routed, *Microprocessor Report*, 4 August 1997. To correct for such unanticipated delays in completing any one microprocessor, Intel's policy is to design several new products in parallel design groups. Development of an alternative product may thus be accelerated through transfers of architectural skills and other resources, to protect the firm's competitive position in given market segments.

<sup>31</sup> Interview, General Manager, California Technology and Manufacturing, 17 December 1998.

**Table 7** Relative performance indicators for the Pentium II microprocessor

<b>Process generation</b>			
Minimum feature-size (microns)	0.35	0.35	0.25
<b>Products</b>			
Brand name	Pentium Pro	Pentium II	
Version	Redesign	Original	Redesign
Date of first shipment	Second quarter, 1996	Second quarter, 1997	Fourth quarter, 1997
<b>Performance indicators</b>			
Die size			
Transistors per microprocessor (millions)	5.5	7.5	7.5
Increase on Pentium Pro product (%)		~36	
Microprocessor die-size (mm <sup>2</sup> )	196	203	131
Die size <i>increase</i> due to architecture enhancement (%)		~4	
Die size <i>reduction</i> due to process generation shift (%)			~35
Die size <i>reduction</i> on joint product & process changes			~33
<b>Clock-speed</b>			
Maximum product clock-speed (MHz)	200	300	450
Speed increment due to product architecture improvement (%)		50	
Speed increment due to process generation shift (%)			50
Speed increment on joint product and process changes (%)			125

*Note:* Intel Corp., *Microprocessor Reference Guide* (2000) and press releases; L. Gwennap and M. Thomsen, *Intel Microprocessor Forecast* (Sebastopol, CA: Micro Design Resources, 1998).

tural improvements alone would have boosted the clock-speed of the Pentium II by ~50 per cent, closely aligning its development and that of the 0.25-micron process resulted in a speed increase of 125 per cent. Complementarities are thus sought through coordinated product and process designs that combine improvements in clock-speed, which increase the marketability of a product, with combined reductions in its die-size that reduce fabrication cost.

However, realizing the incipient benefits of new process and micro-processor generations depends on whether other firms devise more advanced end-user computing devices, and markets for them, so as to accelerate the high-volume deployment of Intel's products. To that end, the firm's executives seek to ensure that their technology roadmap is aligned with those of OEM customers and complementors. It is to these issues that we now turn.

### **Coordination with customers' and complementors' designs**

Since the early 1990s, Intel has taken a direct interest in the formation of end markets for the varied types of products that incorporate its micro-processors. For instance, in the case of a particular version of the Pentium II, the Xeon processor, Intel coordinated its development with that of other firms' workstation and server computers, operating systems, database management systems, and an extensive range of applications software, in such areas as electronic commerce, supply chain management, and mechanical design automation. The aim was to ensure that these firms would invest to 'integrate, tune, and optimize [their] solutions around this new microprocessor',<sup>32</sup> thus expanding Intel's market shares in the enterprise computing segment.

In seeking to align its plans with those of downstream firms, Intel shares elements of its technology roadmap with them, on a reciprocal basis and under non-disclosure agreements, for a period of up to two years prior to the planned product launch dates:

So, about the time that we are freezing on the product that we want to design, and looking forward to two years of design for its introduction, we have to take that to the software community and say 'Fine, here are the 70 new instructions that this processor has which will make [for example] your multi-media applications better', under non-disclosure agreement. 'Here they are, start designing the product'. So, [we take that data to] the software community, and the hardware community, and you also get the [technical analyst] people who make a living out of following our industry...telling them 'this is the direction that Intel's going in'.<sup>33</sup>

The sharing of roadmap data with technical analysts, thus going beyond the firms that are directly involved in product development, is integral

<sup>32</sup> Intel Corporation press release, 'Intel Pentium II Xeon processor launch', 29 June 1998.

<sup>33</sup> Interview, Chief Executive Officer, Intel Corporation, 17 December 1998.

to the coordination of investments at the interfirm level. Bringing about complementary investments at the interfirm level may depend on whether the parties have means of attesting the reliability of each others' claims and promises. In particular, smaller software vendors may be unwilling to invest if they lack confidence in the claims that Intel makes for its future microprocessor generations. As one means of addressing such issues, Intel sometimes provides support in the form of technical assistance and venture capital to such firms.

But, since about 1993, and also to assuage such concerns on the part of downstream firms, Intel has availed of the services of a small number of independent technical analyst firms. One such firm is Micro Design Resources. As its President remarked, 'We are the community organizer. We have brought together this community of people which cares about microprocessors.'<sup>34</sup> What is meant by this is that Micro Design Resources collects information from various parties involved in the production of microprocessors, and disseminates it to the entire network, thus permitting information exchange and informed interaction. Intel informs Micro Design Resources of key technical changes that it plans to incorporate in each of several future products, indicating also the particular market segment to which each one is being addressed, and its expected price point. The analyst firm's income stream depends significantly on the perceived objectivity and accuracy of its appraisals of such microprocessors on the part of customers who buy its newsletters, which include firms throughout the semiconductor, hardware, and software industries, as well as stock analysts. Equally, Intel's willingness to continue sharing data with the analyst firm depends on the latter's adherence to product appraisals that, while they may on occasion be critical, nevertheless adhere to non-disclosure agreements with respect to proprietary data. A technology roadmap thus provides a mechanism for the coordination of investment decisions throughout a design network, extending from suppliers to various sub-units within a firm and to its OEM customers and complementors.

## Conclusions

This chapter has examined the link between capital budgeting and complex organizational strategies. In reporting the results of a field

<sup>34</sup> Interview, President, Micro Design Resources, 7 July 1998.

study of how a major firm in the microprocessor industry coordinates and appraises investments in systems of complementary assets, it has sought to help remedy the deficit in firm-level studies of such issues. We have examined whether managers at Intel systematically coordinate investments in a manner consistent with the theory of complementarities. We have considered the coordination processes and practices that allow integration across sub-units within the firm, and across stages in the design, manufacturing, and marketing processes. We have also shown that capital budgeting and coordination processes can extend beyond the firm in the modern economy. Capital budgeting, we argue, needs to be extended to include a much broader set of processes and issues than has been the case to date. Rather than view this extension as a matter of simply refining valuation methods, the capital budgeting literature needs to accord a central place to the roles of intra- and interorganizational coordination processes in linking the evaluation and management of investment proposals with corporate strategies. The links between investment appraisal and strategy, we argue, need to be taken more seriously by researchers, and their implications for intra- and interorganizational coordination mechanisms considered more extensively.

We have examined a coordination mechanism that has been neglected in the investment appraisal literature in accounting. We have described the overall complementarity structure within which Intel operates, both intra- and interfirm, and demonstrated the costs of failing to coordinate successfully the sets of complementary assets. The role of technology roadmaps in coordinating both investments and expectations has been documented for the sub-units of Intel, and for the relations among Intel and its suppliers, complementors, and OEM customers. The links between roadmaps as coordination mechanisms and traditional capital budgeting practices have also been analysed. We argue that the chapter makes the following three contributions.

First, our findings provide strong firm-level evidence supporting the arguments of Trigeorgis (1995, 1996) and of Milgrom and Roberts (1995*a*, 1995*b*) that the system of assets, rather than the individual investment decision, may often be the critical unit of analysis and decision for managers. This is consistent with intuition and casual observation, and of considerable importance for overall firm strategies. In the case of Intel, analysing 'synergies among parallel projects undertaken simultaneously' (Trigeorgis 1996: 257) is the aspect of investment appraisal that is always considered at the highest levels in the firm because, as we have demonstrated, the costs of failing to coordinate such complementary

investments may be very high. Our findings thus provide support for the extension of theoretical and empirical analyses to incorporate systems of parallel and interacting investment decisions that occur across units within the firm and among firms.

Second, we find that value-maximizing investments in systems of complementary assets require coordination mechanisms that are largely overlooked in recent theoretical literature. In particular, the role of top-level executives extends far beyond Milgrom and Roberts' claim (1995*b*) that they 'need only identify the relevant complementarity structure in order to recommend a "fruitful" direction for coordinated search' to lower-levels in the hierarchy. At Intel, executives have collaborated with peers in supplier, customer, and complementor firms to develop and operationalize a technology roadmap mechanism. We examine how this is used to establish, coordinate, and revise expectations, within and between firms, as to when the components of an asset system should be made available and how they should interoperate to enable system-wide innovation.

In contexts where innovation is widely distributed across sub-units and across firms, the benefits of such a coordination mechanism for dynamically adjusting expectations are particularly significant. As we demonstrate for the case of Intel, decisions on accelerating or postponing investments such as in a new microprocessor are embedded in what one executive termed an 'ecosystem' (Miller and O'Leary 2000). Optimal results may be secured only through awareness of proposed shifts in the time-lines and anticipated outcomes of many other investment decisions, such as made by fabrication process developers within the firm, lithography firms in the supply base, or a set of independent software vendors designing complementary products. To avoid lock-in to an inferior source of component designs, as well as misappropriation of intellectual property, mechanisms for monitoring and evaluating technology development programmes of alternative suppliers are needed. The significance of complementarity relations among investments is widely recognized in the literature, and the merits of identifying such relations at intra- and interfirm levels is also acknowledged. It is important now for researchers to identify and analyse empirically the mechanisms that allow firms to realize the benefits of complementarities.

Third, this study enables us to identify issues for investigation in future large-sample surveys and field-based analyses of the capital budgeting process. In particular, we suggest investigating whether there are systematic differences between industries in the effectiveness

with which interdependent investments are planned and coordinated across firm boundaries. For instance, anecdotal evidence indicates that firms in the telecommunications industry have found it very difficult to align investments in the components of advanced telephony, with significant negative returns to investment as a consequence (Grove 2001). A number of specific research questions follow. For instance, if there are such differences across industries, why do they arise? Are the differences due, for instance, to the absence of appropriate institutional arrangements such as those provided by SEMATECH, or is it attributable to the lack of a norm such as Moore's law, through which initial expectations are formed? Or is it a function of the differing rate and nature of technological progress, such that in one industry (e.g. microprocessors) innovation is relatively predictable and incremental, and in another (e.g. biotechnology) it is highly uncertain and fundamental? Further research should focus on such questions to enable us to ascertain whether there are systematic differences across industries with respect to mechanisms for forming, revising, and enacting expectations, such that some industries are better able to achieve systemic and interfirm innovation than others.

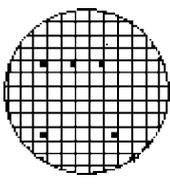
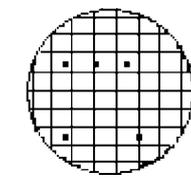
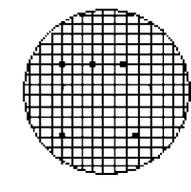
As a result of Graham and Harvey's recent survey (2001), we now have a comprehensive and detailed understanding of the utilization of particular investment valuation practices on the part of large and small firms in a variety of industries. It is important to build upon this information by asking managers whether synergies or complements are addressed formally as part of the capital budgeting process and, if they are, what formal mechanisms are used to achieve this. Our clinical study suggests the widespread use of technology roadmap practices in the computing and microelectronics industries. At Intel, the CEO and other executive officers pay particular attention to investment coordination as a key driver of NPV. This suggests that it is now appropriate for survey researchers to pose questions relating to how the relevant unit of investment analysis and appraisal is arrived at. For instance, a roadmap may offer a robust mechanism for articulating possible responses to the uncertainties of intra- and interfirm coordination. This may be preferable to arbitrarily adjusting the cash flow forecasts or discount rates of individual investment decisions, an approach which Graham and Harvey (2001) observe is presumed in the existing literature. Systematic investigation of these issues, through fieldwork and survey research, would be of considerable benefit.

Additional field studies of the explicit use of formal coordination mechanisms in other industries such as automobile and airplane

manufacture would be extremely valuable. It would be of interest to learn whether mechanisms similar to those observed in the microprocessor industry, which allow for the optimizing of complementary investments, exist in other industries. It would also be of interest to learn how the coordination of expectations is achieved in other industries. While 'Moore's law' sets out a time-line and a corresponding cost improvement for advances in process technology that is specific to the semiconductor industry, it would be helpful to know whether comparable ways of coordinating expectations with respect to investment decisions exist in other industries.

## Appendix

Effects of coordinating a process generation shift with introduction of a new product

Panel A	Panel B	Panel C
Process generation ( $x$ )	Process generation ( $x$ )	Process generation ( $x + 1$ )
Product generation ( $y$ )	Product generation ( $y + 1$ )	Product generation ( $y + 1$ )
		

A microprocessor is fabricated by forming electronic elements, such as transistors, on a square of silicon wafer. The elements are connected by layers of metal traces to form a set of integrated circuits. The finished product is a square of silicon embedded with electronic circuitry, termed a die.

Each square on the circles above represents a microprocessor die fabricated on a silicon wafer, and the black dots represent particles that contaminate the wafer during processing, rendering a microprocessor unusable. It is assumed that the number of particles is a function of imperfections in the fabrication process, and independent of the number of die. Each of the three panels shows a total of five fatal defects in identical locations.

The shift from panel A to panel B shows the effects of introducing a new microprocessor product without a corresponding change in pro-

cess generation. The die-size of product  $(y + 1)$  in panel B is larger than that of its predecessor,  $(y)$  in panel A, because the new microprocessor contains more transistors and circuits to give it added power and functionality. The yield of good-die per wafer is reduced as a consequence: there are fewer dies per wafer, and a greater proportion of them are destroyed by the contaminant particles. Fabrication cost per good (or usable) die will rise as a consequence. Also, the clock-speed of product  $(y + 1)$  may be impaired, because the larger die-size results in electrons travelling longer distances to complete a circuit.

The introduction of the new product  $(y + 1)$  may be more economic if it is coordinated with a process generation change, from  $(x)$  to  $(x + 1)$ , as represented in the shift from panel B to panel C. The increased transistor density provided by the new process will at least partially offset the increased die-size of the new product, such that the yield of good (or usable) die per wafer and the clock-speed of the device are both increased.

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